Electronic Version
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Claims

[c1] 1. A flash memory cell, comprising:
a first conductive type substrate;
a second conductive type first well region configured within the first conductive type substrate;
a stacked gate structure disposed over the first conductive type substrate, wherein the stacked gate structure further comprises a tunneling oxide layer, a floating gate, an inter-gate dielectric layer, a control gate and a cap layer sequentially formed over the first conductive type substrate;
a source region and a drain region configured in the first conductive type substrate on each side of the stacked gate structure;
a first conductive type pocket doped region configured within the second conductive type first well region, wherein the first conductive type pocket doped region extends from the drain region to an area underneath the stacked gate structure close to the source region;
a pair of spacers disposed on the sidewalls of the stacked gate structure;
a first conductive type doped region configured within the drain region such that the first conductive type

doped region extends through a junction between the drain region and the first conductive type pocket doped region, wherein the first conductive type doped region separates from the spacer disposed over the drain region by a distance; and

a contact plug disposed over the drain region and connected electrically with the first conductive type doped region.

[c2] 2. The flash memory cell of claim 1, wherein the first conductive type substrate comprises a p-type substrate.

[c3] 3. The flash memory cell of claim 1, wherein the second conductive type first well region comprises a deep n-well region.

[c4] 4. The flash memory cell of claim 1, wherein the first conductive type pocket doped region comprises a p-type pocket doped region.

[c5] 5. The flash memory cell of claim 1, wherein the first conductive type doped region comprises a p-type doped region.

[c6] 6. The flash memory cell of claim 1, wherein the source region and the drain region are n-type doped regions.

[c7] 7. The flash memory cell of claim 1, wherein the drain

region and the first conductive type pocket doped region are short-circuit connected.

[c8] 8. The flash memory cell of claim 1, wherein the distance separating the first conductive type doped region and the spacer is greater than a depth of the drain region.

[c9] 9. A method of fabricating a flash memory cell, comprising the steps of:
providing a first conductive type substrate;
forming a second conductive type first well region in the substrate;
forming a stacked gate structure over the substrate, wherein the stacked gate structure comprises a tunneling oxide layer, a floating gate, an inter-gate dielectric layer, a control gate and a cap layer sequentially formed over the substrate;
forming a first conductive type pocket doped region in an area of the substrate designated for forming a drain region such that the first conductive type pocket doped region extends to an area underneath the stacked gate structure close to an area designated for forming the a source region;
forming the source region and the drain region in the substrate on each side of the stacked gate structure;
forming a pair of spacers on sidewalls of the stacked gate structure;

forming a first conductive type doped region in the drain region, wherein the first conductive type doped region extends through a junction between the drain region and the first conductive type pocket doped region;
forming an inter-layer dielectric layer over the substrate;
removing a portion of the inter-layer dielectric layer and the spacer to form an contact hole, wherein the contact hole exposes the drain region and the first conductive type doped region such that the first conductive type doped region separates from the spacer by a distance; and
forming a contact plug inside the contact hole, wherein the contact plug is connected to the first conductive type doped region electrically.

[c10] 10. The method of claim 9, wherein the distance separating the first conductive type doped region from the spacer is greater than a depth of the drain region.

[c11] 11. The method of claim 9, wherein the step of forming the first conductive type doped region in the drain region further comprises:
forming a mask layer that exposes the drain region over the substrate;
forming the first conductive type doped region in the substrate on one side of the drain region using the mask layer and the spacer as a self-aligned mask; and

removing the mask layer.

[c12] 12. The method of claim 11, wherein the step of forming the pair of spacers on the sidewalls of the stacked gate structure comprises:
forming first spacers on the sidewalls of the stacked gate structure; and
forming second spacers on the first spacer covered sidewalls of the stacked gate structure.

[c13] 13. The method of claim 12, wherein the first spacers and the second spacers are fabricated with materials having different etching selectivity, and the step of removing a portion of the inter-layer dielectric layer and the spacers to form the contact hole comprises removing a portion of the second spacer so that the first conductive type doped region separates from the second spacer by a distance.

[c14] 14. The method of claim 12, wherein the step of forming the first conductive type doped region in the drain region comprises using the stacked gate structure with the second spacers thereon as a self-aligned mask in an ion implantation process.

[c15] 15. The method of claim 9, wherein the step of forming the first conductive type doped region in the drain re-

gion comprises using the stacked gate structure with the spacers thereon as a self-aligned mask in an ion implantation process.

[c16] 16. The method of claim 11, wherein the step of forming the first conductive type pocket doped region in an area designated form forming the drain region comprises:
forming a first patterned photoresist layer over the substrate, wherein the first patterned photoresist layer exposes the area in the substrate designated for forming the drain region;
performing a first pocket implantation to form the first conductive type pocket doped region in the designated substrate area for forming the drain region; and
removing the first patterned photoresist layer.

[c17] 17. The method of claim 16, wherein the first pocket implantation comprises a tilt angle ion implantation operation.